13. CONTROLS AND MONITORING

13.1. OVERVIEW

Control and monitoring functions for all CMS detector subsystems are co-ordinated by the Detector Control System (DCS) Group in order to design and implement a single control system to operate the detector. Using guidelines provided by DCS, each of the sub-detector groups are to define and design the data acquisition and control function needs for their sub detector. Data from these sub-detectors is available to the global control system which provides console hardware and software, as well as display, archiving and other higher level services. This section describes the control and monitoring of the HCAL sub-detector.

Parameters to be measured by the control system exist in three locations, the counting room, the side galleries of the cavern, and inside the detector itself. Physically, the electronics in the counting room and attached to the forward calorimeter are housed in VMEbus crates. Inside the detector, electronics resides in the readout boxes distributed throughout the HCAL detector. Access to data in the readout boxes will be via a network connection from dedicated DCS crates in the counting room to controller cards in the readout boxes. All VMEbus crates include a DCS processor with a network connection to the higher system levels. The DCS architecture is shown in Fig. 13.1.

13.2 DCS OVERVIEW

13.2.1 Design principles

Hardware architecture

The DCS hardware architecture consists of three principal layers. At the top are operator workstations and general purpose computers which provide access to all of the DCS services. The front-end or bottom layer consists of large number of distributed front-end processors (VME-based). The middle layer is a dedicated local network interfacing the previous layers. This network is segmented for availability purposes, and is connected to the general CERN network by a filtered access. The general CERN connection provides for world wide access by authorised persons. The front-end layer connects to detector systems and equipment through direct I/O or through field buses shows the architecture of the DCS network.

Software architecture

The software architecture is a co-operating network of dedicated control applications, DCS general services and gateways to other CMS and CERN systems. The dedicated control applications are the distributed controls for CMS detectors which are composed of real time process control components and supervision components.

Operations

DCS services are needed for all operational phases of the experiment, from construction and commissioning to physics data taking runs, calibration tests and monitoring during shutdown periods. According to the operational phase, one or more operators will concurrently operate the CMS detector. These operations will be done from control rooms, equipment rooms, or remotely under the filtering of the DCS access control.

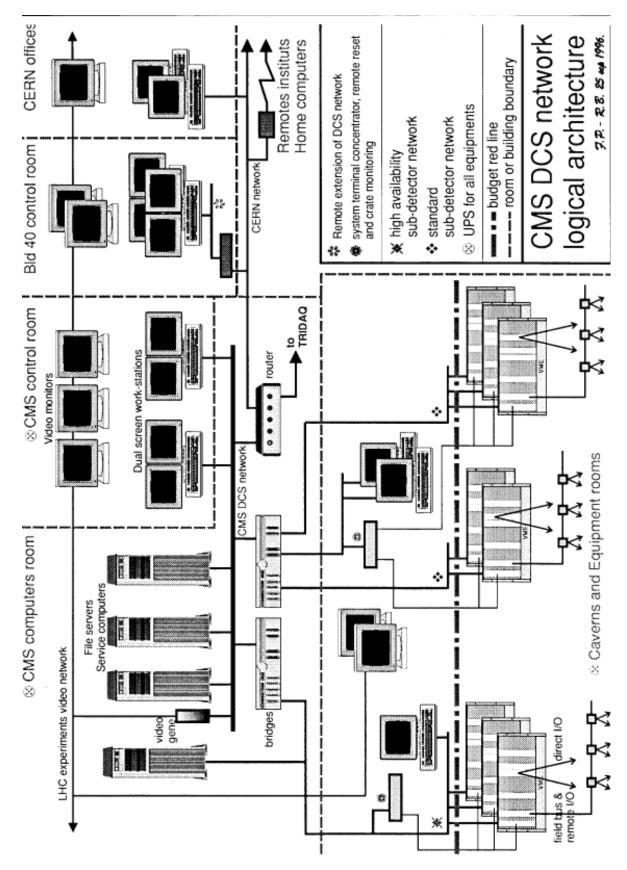


Fig. 13.1: DCS architecture.

DCS toolkit

DCS provides general services; Archiver, Logger, Alarms, Access controls, Central Repository and a manager for the overall DCS activities. A toolkit is provided to build the dedicated control applications at the individual system level. The kit consists of drivers for the commanded I/O hardware, a control kernel, generic applications and a set libraries for specific applications.

13.2.2 Controls software system

The CMS collaboration has decided to implement a common general services software approach using an existing controls package. Commonality among all four LHC experiments is presently under discussion as well. In CMS and ATLAS, the respective DCS groups are evaluating EPICS as a possible general software system and have demonstration projects underway. EPICS is a highly developed software controls system that is widely used in the high energy and nuclear physics community and is supported by many laboratories.

To have a specific configuration and software environment, the remainder of this chapter is based on the use of EPICS in its current VME implementation. In this context, the starting point for the individual detector sub-groups is the EPICS Input-Output-Controller (IOC), a VMEbus based front-end crate containing a single-board computer running EPICS compatible software. At the present time, IOCs use the VxWorks real-time operating system running on Motorola processor boards. The data request protocol, Channel Access (CA) allows upper level processors to read and set parameters in the IOC. At start-up, each IOC is downloaded with the programs and database entries needed to acquire and process locally, the parameters associated with that particular IOC.

Because EPICS is used at many laboratories, software drivers are available for most commercial modules. The DCS group has indicated that they will recommend modules to use for standard analog and digital control system signals. This standardisation goal is intended to minimise the software effort required to implement sub-detector control and monitoring systems.

An important feature of the total EPICS/IOC software package is an extensive system for alarms monitoring and reporting of analog and digital alarm conditions. Included in the alarms task is the provision for two-tier analog alarms, with independent settings for high and low values, plus high-high and low-low values to distinguish severe from off-normal alarm conditions. Using this capability, less severe out-of-tolerance conditions can be reported, allowing preventative maintenance to be performed before real hardware failures occur. Alarm system values are part of the data that is downloaded to each IOC at initialisation time.

In EPICS, the database is a key element that allows the system to be adapted to different applications. Database records that are downloaded to the IOCs are processed at a rate dictated by that record. Processing the record may be as simple as reading an analog value, but other operations such as state machines and PID control loops are also implemented by configuring parameters of predefined database entries rather than writing special programs.

13.3 DISTRIBUTED DATA IN THE HCAL DETECTOR

The majority of the remote data for HCAL consists of readings and settings associated with the HF phototube high voltage supplies and the data channels in the HB and HE sections

of the detector. There are 11,232 data channels distributed over the readout boxes for the barrel and endcap calorimeters. For each of the channels in a given readout box, there are eight bytes of test data, two bytes of timing trim setting data, and a byte of miscellaneous control and mode settings. Also for each readout box, there are about ten voltage and temperature readings to digitise.

To accommodate the above requirements for HB and HE, a small controller card will be added to the card cage used to support the photodetector electronics. This controller card is interfaced to the individual channel ASICs via CAN bus. Support for CAN bus will be included in the channel ASIC. Communication between the readout boxes and the EPICS nodes in the counting room will be by way of fibre optic Arcnet, a small network that can easily provide the necessary data communication requirements. A processor such as the MC68376 can provide the local processing, the CAN bus node interface, the AD converter and operate the Arcnet protocol chip. Inside a readout box, the CAN bus connection could be duplicated or segmented to minimise the effects of any potential single point failure.

From the EPICS VMEbus crates in the counting room, the readout boxes will be star-connected using a commercially available Arcnet copper to fibre optic hub. For convenience, the network cable is to be bundled with the other cables connected from the counting room to the individual readout boxes.

13.3.1 Arcnet

Arcnet is a small local area network that is well matched to the requirements for accessing data in the HCAL readout boxes. Protocol interface chips and network hardware for this LAN are readily available. Arcnet adapters for the counting room nodes are available as VMEbus boards and as IndustryPack modules. Because the readout boxes are inaccessible, the controller cards there should be as simple as possible. One of the important reasons for selecting this network is that very little software is required to support the communications. The protocol supplies secure, acknowledged, collision-free transmission of data frames between nodes with little software overhead.

13.3.2 CAN bus

To conserve backplane space and minimise pin connections, some sort of serial connection is needed to communicate with individual channel ASICs. Instead of developing a non-standard serial connection, the established commercial standard CAN bus will be used. Support for the CAN bus interface can be included in the design of the channel ASIC. During normal operation of the detector, no control system access to the individual channels is needed. At start-up time, the timing delay setting and the mode setting bits are downloaded. For testing purposes, several bytes of test data can be downloaded to each channel. The size of the CAN bus frame is a good match to the needs of the individual channels. A standard CAN bus interface transceiver is used to connect with the backplane of the readout box.

13.3.3 Processor for the readout box controller

The Motorola MC68376 microcontroller will be used for the controller board. This device includes a CAN bus module and a 1-channel 10-bit A-D converter to read the voltages and temperatures within the readout box. These readings will be returned to the EPICS crates in the counting room once a second.

13.3.4 Crate based systems

Control and communication functions for distributed data from detector systems that use standard electronics crates are implemented by providing an EPICS IOC node in each crate.

In the case of readout channels where the CAN protocol is used for communications with the channel ASICs, VME 9U crates are used. The P3 user defined area of the backplane is used for CAN bus lines to each module. Connections back to the higher levels of the DCS are through its standard LAN interfaces.

13.4 VOLTAGES AND CURRENTS

13.4.1 Photodetector high voltage

High voltage supplies for the HCAL photodetectors are commercially available units that reside in the counting room in the case of HB and HE, and in local relay racks for HF. VMEbus-based controllers allow voltage values and maximum current values to be set, read, and alarmed as normal EPICS devices. Control functions for the high voltage channels will include ON, STANDBY, OFF, and the RESET of over-current trips conditions.

Hybrid photodetectors

Hybrid photodetectors (HPD) are used in the barrel and endcap sections of HCAL. There are 36 readout boxes for the barrel section, 36 boxes for the endcap sections, and 72 boxes for the outer calorimeter compartments. The HPDs require an accelerating voltage in the range of 10-16 kV plus a diode bias voltage of 150 volts. There are 144 high voltage supplies, one per readout box, and about 500 bias supplies, one per HPD. These voltages will be cabled separately to each of the boxes. Each supply includes a fast over-current trip. The controllers for the high voltage supplies reside in an EPICS IOC crate. Operating parameters are downloaded as normal EPICS settings.

Photomultiplier tubes

The forward detector uses photomultiplier tubes that require high voltage in the 1-2 kV range. Controllers for the high voltage supplies reside in EPICS IOC crates that are located in racks near the detector. Each supply includes a fast over-current trip. The total number of PMT high voltage channels is 3744. Operating parameters are downloaded as normal EPICS settings.

13.4.2 Front-end electronics power supplies

Voltages are distributed to each readout box separately (chapter 12) where local regulators are used for each channel. Low voltage bulk power supplies, +5V and +10V, for the front end electronics in the readout boxes are located on the side galleries of the cavern. Voltage and current readings for these supplies, both at the source and at the load, along with measurements of the lead temperatures will be returned to IOC crates in the counting house. The forward detector uses standard crate and rack based electronics, and the DCS infrastructure for rack systems can be applied.

13.4.3 Crates and racks

Electronics in the counting room will be implemented in the 9U VME64x format. The design, manufacture, installation, and cooling of the racks and crates is the responsibility of the

CMS infrastructure group. Monitoring and control functions are the province of the DCS group.

The space required to house electronics in the counting room depends on the allowed power dissipation per card. For the case of 16 channels per module and 18 usable slots per crate, the 14,000 readout channels in HCAL will require about 50 crates located in 16 racks. Monitoring operating parameters for each crate is necessary as well as two-tiered alarming on overtemperature, overvoltage or overcurrent conditions.

13.5 TEMPERATURES

Within each of the boxes in the detector, the ambient temperature of the air and the cooling plates will be monitored for alarm conditions. In this case, no additional control is needed, because the reason for an alarm condition can usually not be corrected by the HCAL group. Temperature readings would be returned to the IOC crates in the counting room using the Arcnet connection to the individual boxes. Temperature monitoring and alarming for the forward calorimeter rack systems are included in the standard rack protection package.

13.6 SOURCE CALIBRATION

A source calibration system is integrated into the HCAL sub detector. A radioactive source attached to a wire is guided by a small tube through portions of the detector while the DC response of the scintillator, light pipe, and photodetector system is recorded using the normal fast data collection system. Control is needed to select between several tubes and to drive the wire out and back during this calibration process. Twenty four such calibration systems are needed to cover all parts of the HCAL system. The source motion can be controlled either by the processor in the IOC crate, or by a companion processor board in the IOC crate. To interpret the calibration data, the source position must be correlated with the response data from the photodetectors. Even without a special timing system, measurements in separate EPICS IOCs can be correlated to a few milliseconds.

For the calibration process, the front-end electronics will be downloaded with parameters such that 16 consecutive readings are summed by the FIR filter of the second level trigger electronics. Then several hundred such sums will be averaged and the results correlated with the position of the source. Both the front-end electronics crate and the source controller crates will contain an EPICS CPU card. The reading of source calibration data will be controlled by the EPICS processor in the front-end crate which is able to cause the Level_1_Accept trigger needed to control the second level filter. This EPICS node will request and receive time-stamped values of source position from the EPICS CPU in the source controller crate. It is desirable to have the calibration system independent of the Data Acquisition System and so the processing of the calibration data is done by the EPICS system in the front-end electronics crate. It is not necessary for the trigger and DAQ systems to be operating during source calibration operations, only the system clock is needed. Details of the source controllers, the mechanism for moving the source and the readout of source position are described in chapter 10.

13.7 LUMINOSITY MONITOR

Part of the Luminosity monitor instrumentation includes several Roman Pots which contain devices that measure small angle scattered particles near the beam. In addition to the front-end electronics used to process the detector data, the Roman Pots need slow controls support for motor drivers, position readouts, high voltage control and readout, and downloading operating parameters and test patterns. Front-end data processing electronics will reside in two VMEbus crates, and to provide the slow controls support, an EPICS IOC processor will also reside in each of these crates. These processors are also used to read and monitor the parameters for the Roman Pots and provide an access filtered path for authorised personnel (in the accelerator control room) to read and control the position of moveable devices near the beam.

13.8 ARCHIVES

The upper levels of DCS will provide archived information for HCAL. Two types of archives are needed; constants used for calibration and configuration of the detector, and values of monitored parameters. Values include voltage and current readings, temperature measurements, and results of calibration runs.

13.9 TESTING FACILITIES

Test capability will be needed for the front-end DAQ and trigger electronics located in the counting room. It is expected that boundary scan testing will be incorporated into the design of the digital electronics. All electronics in the counting room will reside in VMEbus crates, so test data and readback will be possible over the DCS network. Test events can be written to and read back from the DAQ buffers using EPICS software in a processor located in each crate.

Operational testing and troubleshooting should be possible to accomplish from a remote workstation, located anywhere. Real-time, or pseudo real-time, correlated displays of accelerator data, detector data, and DCS parameter values are essential for diagnostics and troubleshooting. Gateways to the data acquisition processor farm and to the accelerator Controls System should offer this functionality.

TABLE OF CONTENTS

13.1. OVERVIEW	498
13.2 DCS OVERVIEW	498
13.2.1 DESIGN PRINCIPLES	498
13.2.2 Controls software system.	500
13.3 DISTRIBUTED DATA IN THE HCAL DETECTOR	500
13.3.1 Arcnet	501
13.3.2 CAN BUS	501
13.3.3 Processor for the readout box controller	501
13.3.4 Crate based systems	502
13.4 VOLTAGES AND CURRENTS	502
13.4.1 Photodetector high voltage	502
13.4.2 Front-end electronics power supplies	502
13.4.3 Crates and racks	502
13.5 TEMPERATURES	503
13.6 SOURCE CALIBRATION	503
13.7 LUMINOSITY MONITOR	504
13.8 ARCHIVES	504
13.9 TESTING FACILITIES	504